CLAIMS

1. A method of forming a semiconductor structure comprising:
etching through a nitride layer;
etching through an oxide layer; and
etching a semiconductor substrate; wherein:
a last portion of the nitride layer is etched with a nitride etching chemistry comprising a fluorinated hydrocarbon, oxygen, and an inert gas selected from the group consisting of neon, argon, krypton, xenon, and combinations thereof;
a last portion of the oxide layer is etched with an oxide etching chemistry that is different from the nitride etching chemistry; and
the nitride layer is on the oxide layer, and the oxide layer is on the semiconductor substrate.

2. The method of claim 1 wherein an antireflective coating is on the nitride layer, and wherein the method further comprises etching the antireflective coating using the nitride etching chemistry.

3. The method of claim 1 further comprising overetching the nitride layer using the nitride etching chemistry by up to and including ten percent of the nitride end point.

4. The method of claim 1 wherein the fluorinated hydrocarbon is selected from the group consisting of CF_4, CHF_3, CH_2F_2, CH_3F, and combinations thereof.

5. The method of claim 1 wherein the oxide etching chemistry comprises a fluorinated hydrocarbon selected from the group consisting of CF_4, CHF_3, CH_2F_2, CH_3F, and combinations thereof.

6. The method of claim 5 wherein the semiconductor substrate comprises silicon, and wherein the etching of the semiconductor substrate is achieved with a silicon etching chemistry comprising a reagent selected from the group consisting of a halogen gas, a hydrogen halide, oxygen, and combinations thereof.

7. The method of claim 5 wherein the oxide etching chemistry comprises CF_4 and CHF_3.

8. The method of claim 7 wherein a ratio of CF_4 flow rate to CHF_3 flow rate ranges from one to one up to and including one to six.

9. The method of claim 6 wherein the silicon etching chemistry comprises Cl_2, HBr, and O_2.

10. The method of claim 1 wherein the nitride etching chemistry comprises CF_4, CHF_3, Ar, and O_2.

11. The method of claim 10 wherein a ratio of CF_4 flow rate to CHF_3 flow rate varies from six to one down to and including one to one.

12. The method of claim 1 wherein the nitride etching chemistry is introduced with a bias of at least –50 V.

13. The method of claim 1 wherein a ratio of pressure:top power:bias of the nitride etching chemistry is 1-50 mTorr:100-750 W:–50—500 V.

14. The method of claim 10 wherein a ratio of pressure:top power:bias of the nitride etching chemistry is 1-50 mTorr:100-750 W:–50—500 V.

15. The method of claim 7 wherein a ratio of CF_4 flow rate:CHF_3 flow rate is 1-500 sccm:5-500 sccm.

16. The method of claim 6 further comprising cleaning the semiconductor substrate with a silicon cleaning chemistry comprising a fluorinated hydrocarbon and an inert gas selected from the group consisting of neon, argon, krypton, xenon, and combinations thereof.

17. The method of claim 6 further comprising cleaning the semiconductor substrate using a silicon cleaning chemistry comprising CF_4 and argon.

18. The method of claim 23 wherein the silicon cleaning chemistry is introduced with a bias of at least –50 V.

19. A method of forming a semiconductor structure comprising:
etching through a nitride layer;
etching through an oxide layer; and

etching a semiconductor substrate, which comprises silicon;

wherein:

a last portion of the nitride layer is etched with a nitride etching chemistry comprising CF_4, CHF_3, Ar, and O_2;

a last portion of the oxide layer is etched with an oxide etching chemistry comprising CF_4 and CF_3;

the semiconductor substrate is etched with a silicon etching chemistry comprising Cl_2, HBr, and O_2; and

the nitride layer is on the oxide layer, and the oxide layer is on the semiconductor substrate.

20. A method of making a semiconductor device comprising:

making a semiconductor structure by the method of claim 1; and

forming a semiconductor device from the structure.

21. A method of making an electronic device comprising:

making a semiconductor device by the method of claim 20; and

forming an electronic device, which comprises the semiconductor device.

22. A method of making a semiconductor device comprising:

making a semiconductor structure by the method of claim 19; and

forming a semiconductor device from the structure.

23. A method of making an electronic device comprising:

making a semiconductor device by the method of claim 22; and

forming an electronic device, which comprises the semiconductor device.

24. A silicon wafer comprising a plurality of semiconductor structures produced by the method of claim 1.

25. A silicon wafer comprising a plurality of semiconductor structures produced by the method of claim 19.

26. A silicon wafer comprising at least one trench having rounded top corners and rounded bottom corners, wherein the trench comprises a semiconductor structure produced by the method of claim 1.

27. A silicon wafer comprising at least one trench having rounded top corners and rounded bottom corners, wherein the trench comprises a semiconductor structure produced by the method of claim 19.

28. A silicon wafer comprising at least one isolation region, wherein the isolation region comprises a trench, and wherein the trench comprises a dielectric material and a semiconductor structure produced by the method of claim 1.

29. A silicon wafer comprising at least one isolation region, wherein the isolation region comprises a trench, and wherein the trench comprises a dielectric material and a semiconductor structure produced by the method of claim 19.

30. A method of forming a trench having reduced defects comprising:

etching through a nitride layer;

etching through an oxide layer; and

etching a semiconductor substrate; wherein:

a last portion of the nitride layer is etched with a nitride etching chemistry comprising a fluorinated hydrocarbon, oxygen, and an inert gas selected from the group consisting of neon, argon, krypton, xenon, and combinations thereof;

a last portion of the oxide layer is etched with an oxide etching chemistry that is different from the nitride etching chemistry;

the nitride layer is on the oxide layer, and the oxide layer is on the semiconductor substrate; and

the trench is formed by the etching of the semiconductor substrate.